AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A method of manufacturing a semiconductor integrated circuit having a first circuit region using a first power supply voltage and a second circuit region using a second power supply voltage different from said first power supply voltage wherein:

a first design rule is applied to said first circuit region in accordance with said first power supply voltage; and

a second design rule is applied to said second circuit region in accordance with said second power supply voltage;

wherein a wiring interval of said first circuit region is determined as a minimum distance allowing a first breakdown voltage of said first design rule; and

wherein a wiring interval of said second circuit region is determined as a minimum distance allowing a second breakdown voltage of said second design rule.

Claim 2 (Canceled).

Claim 3 (Currently Amended): ~~The method of manufacturing the semiconductor integrated circuit as claimed in claim 1,~~ A method of manufacturing a semiconductor integrated circuit having a first circuit region using a first power supply voltage and a second circuit region using a second power supply voltage different from said first power supply voltage wherein:

a first design rule is applied to said first circuit region in accordance with said first power supply voltage; and

a second design rule is applied to said second circuit region in accordance with said second power supply voltage;

wherein a distance between adjacent two vias formed in said first circuit region is determined as a minimum distance allowing a first breakdown voltage of said first design rule; and

wherein a distance between adjacent two vias formed in said second circuit region is determined as a minimum distance allowing a second breakdown voltage of said second design rule.

Claim 4 (Original): The method of manufacturing the semiconductor integrated circuit as claimed in claim 3, wherein:

said distance between the adjacent two vias formed in said first circuit region is the shortest distance therebetween; and

said distance between the adjacent two vias formed in said second circuit region is the shortest distance therebetween.

Claim 5 (Currently Amended): ~~The method of manufacturing the semiconductor integrated circuit as claimed in claim 1,~~ A method of manufacturing a semiconductor integrated circuit having a first circuit region using a first power supply voltage and a second circuit region using a second power supply voltage different from said first power supply voltage wherein:

a first design rule is applied to said first circuit region in accordance with said first power supply voltage; and

a second design rule is applied to said second circuit region in accordance with said second power supply voltage;

wherein a distance between adjacent wiring groove and via formed in said first circuit region is determined as a minimum distance allowing a first breakdown voltage of said first design rule; and

wherein a distance between adjacent wiring groove and via formed in said second circuit region is determined as a minimum distance allowing a second breakdown voltage of said second design rule.

Claim 6 (Original): The method of manufacturing the semiconductor integrated circuit as claimed in claim 5, wherein:

said distance between the adjacent wiring groove and via formed in said first circuit region is the shortest distance therebetween; and

said distance between the adjacent wiring groove and via formed in said second circuit region is the shortest distance therebetween.

Claim 7 (Original): The method of manufacturing the semiconductor integrated circuit as claimed in claim 1, wherein said semiconductor integrated circuit employs a Dual-Damascene process to form metal wirings of said first and second circuit regions.

Claim 8 (Original): The method of manufacturing the semiconductor integrated circuit as claimed in claim 7, wherein said metal wirings are copper wirings.

Claim 9 (Currently Amended): A semiconductor integrated circuit having a first circuit region using a first power supply voltage and a second circuit region using a second power supply voltage different from said first power supply voltage wherein:

said first circuit region is manufactured by a first design rule in accordance with said first power supply voltage; and

said second circuit region is manufactured by a second design rule in accordance with said second power supply voltage;

wherein said first circuit region has a first wiring interval corresponding to a minimum distance allowing a first breakdown voltage of said first design rule; and

wherein said second circuit region has a second wiring interval corresponding to a minimum distance allowing a second breakdown voltage of said second design rule.

Claim 10 (Canceled).

Claim 11 (Currently Amended): ~~The semiconductor integrated circuit as claimed in claim 9,~~ A semiconductor integrated circuit having a first circuit region using a first power supply voltage and a second circuit region using a second power supply voltage different from said first power supply voltage wherein:

said first circuit region is manufactured by a first design rule in accordance with said first power supply voltage; and

said second circuit region is manufactured by a second design rule in accordance with said second power supply voltage;

wherein said first circuit region has a first distance between adjacent two vias formed in said first circuit region corresponding to a minimum distance allowing a first breakdown voltage of said first design rule; and

wherein said second circuit region has a second distance between adjacent two vias formed in said second circuit region corresponding to a minimum distance allowing a second breakdown voltage of said second design rule.

Claim 12 (Original): The semiconductor integrated circuit as claimed in claim 11, wherein:

said first distance is the shortest distance between the adjacent two vias formed in said first circuit region; and

said second distance is the shortest distance between the adjacent two vias formed in said second circuit region.

Claim 13 (Currently Amended): ~~The semiconductor integrated circuit as claimed in claim 9,~~ A semiconductor integrated circuit having a first circuit region using a first power supply voltage and a second circuit region using a second power supply voltage different from said first power supply voltage wherein:

said first circuit region is manufactured by a first design rule in accordance with said first power supply voltage; and

said second circuit region is manufactured by a second design rule in accordance with said second power supply voltage;

wherein said first circuit region has a first distance between adjacent wiring groove and via formed in said first circuit region corresponding to a minimum distance allowing a first breakdown voltage of said first design rule; and

wherein said second circuit region has a second distance between adjacent wiring groove and via formed in said second circuit region corresponding to a minimum distance allowing a second breakdown voltage of said second design rule.

Claim 14 (Original): The semiconductor integrated circuit as claimed in claim 13, wherein:

said first distance is the shortest distance between the adjacent wiring groove and via formed in said first circuit region; and

said second distance is the shortest distance between the adjacent wiring groove and via formed in said second circuit region.

Claim 15 (Original): The semiconductor integrated circuit as claimed in claim 9, wherein said semiconductor integrated circuit employs a Dual-Damascene process to form metal wirings of said first and second circuit regions.

Claim 16 (Original): The semiconductor integrated circuit as claimed in claim 15, wherein said metal wirings are copper wirings.

Claim 17 (New): The method of manufacturing the semiconductor integrated circuit as claimed in claim 3, wherein said semiconductor integrated circuit employs a Dual-Damascene process to form metal wirings of said first and second circuits.

Claim 18 (New): The method of manufacturing the semiconductor integrated circuit as claimed in claim 17, wherein said metal wirings are copper wirings.

Claim 19 (New): The method of manufacturing the semiconductor integrated circuit as claimed in claim 5, wherein said semiconductor integrated circuit employs a Dual-Damascene process to form metal wirings of said first and second circuit regions.

Claim 20 (New): The method of manufacturing the semiconductor integrated circuit as claimed in claim 19, wherein said metal wirings are copper wirings.

Claim 21 (New): The semiconductor integrated circuit as claimed in claim 11, wherein said semiconductor integrated circuit employs a Dual-Damascene process to form metal wirings of said first and second circuit regions.

Claim 22 (New): The asemiconductor integrated circuit as claimed in claim 21, wherein said metal wirings are copper wirings.

Claim 23 (New): The semiconductor integrated circuit as claimed in claim 13, wherein said semiconductor integrated circuit employs a Dual-Damascene process to form metal wirings of said first and second circuit regions.

Claim 24 (New): The semiconductor integrated circuit as claimed in claim 23, wherein said metal wirings are copper wirings.